REMARKS

In the Official Action, the Examiner rejected all pending claims 1-12. In the present response, Applicants have amended claims 1, 7 and 12 to clarify the claimed subject matter. Reconsideration of the Application in view of the remarks set forth below is respectfully requested.

Rejection Under 35 U.S.C. § 102

The Examiner rejected claims 1, 3-6 and 8-11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,192,883 , herein after referred to as "the Kimura reference." Specifically, the Examiner stated:

> Claims 1, 3-6, and 8-11 are rejected under 35 U.S.C. 102 (b) as being anticipated by Kimura (US Pat 5,192,883).
>
> Regarding **claims 1 and 6,** Kimura discloses a system, comprising:
>
> a processor (col. 4, lines 28-34, un-shown CPU);
>
> a power supply coupled to the processor (col. 2, line 57-col. 3, line 13, as power supply is present in the system, which is inherently supplying power to all the active components, including a CPU); and
>
> a device (fig. 5, 150) coupled to the processor and the power supply and comprising:
>
> an internal power supply bus configured to receive a power signal from the power supply (fig. 5, Vc); and
>
> an isolation circuit (fig. 5, 102) configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit (fig. 5, control signal VBC when being low turn isolation transistor 102 off, col.1, lines 20-33, '... transistor 102 adapted to connect/cut off the supply voltage Vc).
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> Official Action mailed July 27, 2004, pp. 2-3 (Emphasis in original).

Applicants respectfully assert that the Kimura reference does not anticipate the claimed subject matter. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application is directed to a technique for implementing a zero power standby mode with reduced leakage current. In operating electronic devices, a standby mode or a sleep state is typically implemented to maintain power to certain components when the system is not in use. Typical electronic devices lose some leakage current even though they are in a standby mode or a sleep state. *See* Application, p. 3, lines 15-22. To prevent or further reduce the leakage currents in the standby mode, an isolation circuit in accordance with embodiments of the present invention may be implemented. *See* Application, p. 6, line 21-p. 7, line 3. The isolation circuit, which may be activated by a control signal, may be used to disconnect an internal power supply bus from an external voltage source to reduce leakage currents in response to initiating a standby mode. *See* Application, p. 9, lines 3-9; p. 9, lines 15-27; p. 10, line 25 – p. 11, line 7. However, circuitry in the memory device may continue to receive power regardless of the mode indicated by the control signal. *See* Application, page 11, line 21- page 12, line 7. Specifically, claim 1 recites "an isolation circuit configured to disconnect the internal power supply bus from the

power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit" and "circuitry coupled to the pad and isolation circuit and configured to receive the power signal regardless of the standby mode indicated by the control signal."

In contrast, the Kimura reference describes an interface circuit for a semiconductor memory device. *See* Kimura, col. 1, lines 7-12. This interface circuit 151, which is part of a device 150, is detachably connected to a memory device 101. *See id.* at col. 1, lines 20-25. The interface circuit 151 has a transistor 102 coupled between a supply voltage Vc and a power supply terminal Vcc of the memory device 101. *See id.* at col. 1, lines 30-53. The transistor 102 is controlled by a power supply/bus control signal VBC. *See id.* This power supply/bus control signal VBC either closes the transistor 102 to provide power for the memory device 101 or opens the transistor 102 to prevent power from being provided to the memory device 101. As such, the reference simply relates to an *external* circuit that interfaces with the memory device to provide power or to isolate the memory device 101 from power.

In the rejection, the Examiner asserted that the Kimura reference discloses all of the claimed subject matter. Specifically, the Examiner asserted that the power supply/bus control signal VBC of Kimura corresponds to the "control signal" of the claims, that the transistor 102 of Kimura corresponds to the "isolation circuit" of the claims, that power supply Vc of Kimura corresponds to the "power supply" of the claims, and that the Vc' of Kimura corresponds to the "internal power bus" of the claim. However, despite the Examiner's foregoing assertions, the Kimura reference fails to anticipate the claims. For example, the Kimura reference fails to

disclose a device having "circuitry coupled to the pad and isolation circuit and configured to receive the power signal regardless of whether the standby mode is indicated by the control signal," as recited in claim 1. Hence, Applicants respectfully submit that the Kimura reference fails to disclose the claimed subject matter, as discussed below.

To begin, the Kimura reference fails to disclose "circuitry coupled to the pad and isolation circuit and configured to receive the power signal regardless of the standby mode indicated by the control signal," as recited in claim 1. As noted above, the Examiner asserted that the transistor 102 corresponds to the "isolation circuit" and that the power supply/bus control signal VBC corresponds to the "control signal." In Kimura, the transistor 102 is coupled between a supply voltage Vc and a power supply terminal Vcc of the memory device 101. *See* Kimura, Fig. 5, col. 1, lines 30-53. The transistor 102, which is part of the device 150, is external to the memory device 101. *See id.* The transistor 102 provides the supply voltage Vc based on a power supply/bus control signal VBC that is provided to the transistor 102. *See* is. at col. 2, lines 27- 33. No power signal is provided to any part of the device 150 or memory device 101 without the transistor 102 receiving a high-level power supply/bus control signal VBC. Clearly, the Kimura reference does not disclose providing power to circuitry in the device *regardless* of whether the standby mode is indicated by the control signal. As such, the transistor 102 is incapable of disconnecting an internal power supply bus of the device, while power is provided to circuitry in the device. Accordingly, Kimura cannot possibly disclose "circuitry coupled to the pad and isolation circuit and configured to receive the power signal regardless of whether the standby mode is indicated by the control signal," as further recited in claim 1.

For at least the reasons set forth above, it is clear that the Kimura reference fails to disclose all the recited features of the instant claims and thus, cannot possibly anticipate the claimed subject matter. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1, 3-6 and 8-11.

First Rejection Under 35 U.S.C. § 103

The Examiner rejected claim 2 under 35. U.S.C. § 103 (a) as being unpatentable over Kimura in view of U.S. Pat. No. 5,638,330, which is herein after referred to as "the Confalonieri reference." Applicants respectfully traverse this rejection.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

Claim 2 depends from independent claim 1 and is believed to be patentable based upon this dependency. In the rejection, the Examiner admitted that the Kimura reference does not

disclose the system being a cellular phone. In an attempt to remedy this deficiency, the Examiner relied upon the Confalonieri reference to disclose the feature. However, the Confalonieri reference describes a low dissipation initialization circuit that is useful with memory registers. *See* Confalonieri, col. 1, lines 6-9. In Confalonieri, problems with power consumption in a power-down condition mean that power consumption should be close to zero. *See* Confalonieri, col. 2, lines 53-60. However, the Confalonieri reference does not disclose or suggest a device comprising an isolation circuit that isolates an internal power bus and also having circuitry that receives power signals regardless of whether the standby mode is indicated by the control signal. As such, the Confalonieri reference does not cure the deficiencies of the Kimura reference, which are discussed above. Therefore, claim 2 is patentable by virtue of its dependence on independent claim 1. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claim 2.

Second Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 7 and 12 under 35. U.S.C. § 103(a) as being unpatentable over Kimura in view of U.S. Pat. No. 5,117,129, which is herein after referred to as "the Hoffman reference." Applicants respectfully traverse this rejection.

Claims 7 and 12 depend from independent claim 1 and are believed to be patentable based on this dependence. In the rejection, the Examiner admitted that the Kimura reference fails to disclose an isolation circuit coupled between a pad on the device configured to receive the power signal and the internal power supply bus, and an I/O pad and circuitry coupled between the output buffer and the I/O pad to tri-state the I/O pad, as recited in claims 7 and 12. The

Examiner relied on the Hoffman reference to disclose these recited features. However, the Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See* Hoffman, col. 1, lines 36-39. Specifically, the reference describes a CMOS circuit that presents high impedance when the voltage V_{DD} is equal to ground. *See* Hoffman, col. 3, lines 1-5 and 37-56. In the Hoffman reference, the pad signal 150 is coupled to the I/O pad 152 through a circuit, which includes various transistors and logic devices. *See* Hoffman, Fig. 3A, col. 3, lines 25-30. Thus, the operation of the circuit is not based on a *control signal that indicates a standby-mode*, but rather is based on the voltage V_{DD}. *See*, Hoffman, col. 3, lines 36-56. Further, the Hoffman reference does not disclose or suggest a device comprising an isolation circuit that isolates an internal power bus and also having circuitry that receives power signals regardless of whether the standby mode is indicated by the control signal. As such, the Hoffman reference does not cure the deficiencies of the Kimura reference, which are discussed above. Therefore, claims 7 and 12 are patentable at least by virtue of their dependence on independent claim 1. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 7 and 12.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 1-12. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

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Robert A. Manware
Reg. No. 48,758
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545